and right quadrants) times the number of I/O lines in the bus to each subarray quadrant (8 lines each times 4=32 lines in the preferred implementation). Finally, during each RAS cycle, two different subarrays, e.g. 157 and 153, are accessed. This doubles again the available number of I/O lines containing data. Taken together, these changes increase the internal I/O bandwidth by at least a factor of 8. Four internal buses are used to route these internal I/O lines. Increasing the number of I/O lines and then splitting them in the middle greatly reduces the capacitance of each internal I/O line which in turn reduces the column access time, increasing the column access bandwidth even further.

IN THE CLAIMS:

Please **substitute** the following claims for the pending claims having the same claim number:

(A version with markings to show changes made to the claims is attached as Exhibit A)

1   173. (Amended) A synchronous memory device including an array of

2   memory cells, the synchronous memory device comprises:

3   clock receiver circuitry to receive an external clock signal;

4   input receiver circuitry to sample a first operation code

5   synchronously with respect to a transition of the external clock

6   signal; and

7   a programmable register to store a binary value, wherein the

8   memory device stores the binary value in the programmable register in

9   response to the first operation code.

1   174. (Amended) The memory device of claim 173 wherein the binary

2   value is representative of a number of clock cycles of the external

3   clock signal to transpire before the memory device outputs data AND

4   wherein the memory device outputs data in response to a second

5   operation code.

1   176. (Amended) The memory device of claim 175 wherein the output

2   driver circuitry outputs a first portion of the data synchronously with

3   respect to a rising edge transition of the external clock signal and a

4   second portion of the data synchronously with respect to a falling edge

5   transition of the external clock signal.

Please **ADD** the following claims:

1   181. (New) The method of claim 151 wherein the first operation

2   code is sampled from an external bus.

1   182. (New) The method of claim 181 wherein the external bus

2   includes a plurality of signal lines and wherein the binary value and

3   the first operation code are multiplexed over the plurality of signal

4   lines.

1   183. (New) The method of claim 164 wherein the first operation

2   code is issued to an external bus.

1   184. (New) The method of claim 183 wherein the external bus

2   includes a plurality of signal lines and wherein the binary value and

3   the first operation code are multiplexed over the plurality of signal

4   lines.

1   185. (New) The memory device of claim 173 wherein the array of

2   memory cells includes dynamic random access memory cells.

1   186. (New) The memory device of claim 173 wherein the input

2   receiver circuitry samples the first operation code from an external

3   bus.

1   187. (New) The memory device of claim 186 wherein the external bus

2   includes a plurality of signal lines and wherein the first operation

3   code and the address information are multiplexed over the plurality of

4   signal lines.

188. (New) The memory device of claim 187 wherein data, the first operation code and the address information are multiplexed over the plurality of signal lines.